IN THE CLAIMS

1. (Currently Amended) An authentication communicating semiconductor device, comprising:

~~a semiconductor chip;~~

a main processing unit ~~formed on said semiconductor chip~~ for generating a first key code according to a predetermined algorithm, for determining approval/non-approval of communication of data with an external device, and for controlling ~~the~~ said communication of data;

an encryption unit ~~formed on said semiconductor chip~~ for encrypting ~~and decoding~~ communication data to transmit to outside using said first key code generated by said main processing unit;

a first interface unit ~~formed on said semiconductor chip~~ for ~~conducting~~ performing first communication with an upper layer according to a first predetermined protocol; and

a second interface unit ~~formed on said semiconductor chip~~ for ~~conducting~~ performing second communication with a lower layer according to a second predetermined protocol,

wherein said main processing unit, said encryption unit, said first interface unit and said second interface unit are formed on a semiconductor chip,

wherein said encryption unit uses communication data received from an outside device using a second key code generated by said outside device,

wherein each of a standard of said first interface unit and a standard of said second interface unit is of a predetermined standard,

wherein said main processing unit, said encryption unit, and said first and second interface units are coupled to each other via an internal bus.

2. (Currently Amended) ~~An~~ The authentication communicating semiconductor device according to claim 1, wherein said main processing unit comprises:

a nonvolatile memory having stored therein a program implementing a key generation algorithm and an authentication algorithm to authenticate ~~an~~ said communication of data in connection with said external device by said external device requesting ~~data communication~~ said communication of data;

~~program-execution-type control means~~ a central processing unit for generating ~~a~~ said first key code and for determining said approval/non-approval of said communication of data with ~~an~~ said external device according to ~~the~~ said program; and

a volatile memory for providing a work area for said ~~control means~~processing unit,

said nonvolatile memory, said ~~control means~~ central processing unit, said volatile memory, said encryption unit, and said first and second interface units being ~~connected~~ coupled to each other via ~~an~~ said internal bus.

3. (Currently Amended) ~~An~~ The authentication communicating semiconductor device according to claim 2, wherein:

said encryption unit includes a first register to which ~~the~~ said first key code generated by said main processing unit is set; and

said encryption unit encrypts ~~and decodes~~ said communication data to transmit to said external device according to ~~the~~ said first key code set via said internal bus

to said first register,

wherein said encryption unit decodes said communication data received from said external device according to said second key code set via said internal bus to said first register.

4. (Currently Amended) ~~An~~ The authentication communicating semiconductor device according to claim 3, wherein:

each of said first and second interface units includes a second register to which a communication code is set; and

said ~~each interface unit conducts~~ first interface unit performs said first communication according to a first communication control code set by said main processing unit via said internal bus to said second register of said first interface unit,

said second interface unit performs said second communication according to a second communication control code set by said main processing unit via said internal bus to said second register of said second interface unit.

5. (Currently Amended) ~~An~~ The authentication communicating semiconductor device according to claim 4, further comprising an external terminal coupled with said internal bus.

6. (Currently Amended) An electronic device, comprising:

an authentication communicating semiconductor device according to claim 5; and

an external memory ~~connected~~ coupled to said external terminal ~~connect~~ which is coupled to said internal bus, wherein:

a communication control program which includes a predetermined program for setting of a communication path is stored in said external memory; and

said main processing unit sets, according to said communication control program, ~~a~~ said first communication control code to said second register of ~~said each interface section~~ said first interface unit to ~~conduct~~ perform said first communication with an external device and said second

communication control code to said second register of said second interface unit to perform said second communication with an external device.

7. (Currently Amended) An authentication communicating semiconductor device, comprising:

~~a single semiconductor chip;~~

an encryption unit ~~formed on said single semiconductor chip~~ for encrypting, in an encrypting mode, ordinary ~~or non-encrypted statement~~ data into encrypted ~~statement~~ data; for decoding, in a decoding mode, ~~the~~ said encrypted ~~statement~~ data into said ordinary ~~statement~~ data; and for directly passing data therethrough when neither encryption nor decoding is required;

a lower-layer interface unit ~~formed on said single semiconductor chip~~ for ~~the~~ said encrypted ~~statement~~ data of said encryption unit for controlling a first protocol of communication with a lower layer;

an upper-layer interface unit ~~formed on said single semiconductor chip~~ for ~~the~~ said ordinary ~~statement~~ data of said encryption unit for controlling a second protocol of

communication with an upper layer; and

a key generation unit ~~formed on said single semiconductor chip~~ for executing authentication processing of communication passing through ~~the~~ said lower layer and for executing key generation processing for said encryption unit, wherein:

said lower-layer interface unit comprises ~~at least one~~ a lower-layer communication path for communicating said encrypted ~~statement~~ data with a lower-layer device controlling a communication signal outside said semiconductor chip;

said upper-layer interface unit comprises ~~at least one~~ an upper-layer communication path for communicating said ordinary ~~statement~~ data with an upper-layer device outside said semiconductor chip; and

said key generation unit comprises a CPU, ~~an~~ a ROM, and ~~an~~ a RAM~~; and~~

~~said CPU sets a key register for said encryption unit to hold an encryption key, a control register of said lower-layer interface unit, and a control register of said upper-layer interface unit via a bus connecting said CPU, said encryption unit, said lower-layer interface unit, and said~~

~~upper-layer interface unit to each other~~.

8. (Currently Amended) ~~An~~ The authentication communicating semiconductor device according to claim 7, further comprising:

a first ~~upper-layer-lower-layer~~ communication path and a second ~~upper-layer-lower-layer~~ communication path between said lower-layer interface unit ~~to~~ and said upper-layer interface unit without passing said encryption unit,

said upper-layer interface unit comprising a first upper-layer communication path and a second upper-layer communication path for communicating signals with ~~an~~ said upper-layer device outside said semiconductor chip,

said first upper-layer communication path being capable of selecting data from said encryption unit and data from said lower-layer interface unit without passing through said encryption unit,

said second upper-layer communication path being capable of selecting data from said first ~~upper-layer-lower-layer~~ communication path and data from said second ~~upper-layer-lower-layer~~ communication path.

9. (Currently Amended) ~~An~~ The authentication communicating semiconductor device according to claim 7, wherein:

said encryption unit comprises a first encryption circuit and a second encryption circuit; ~~and~~

said upper-layer interface unit includes a first upper-layer interface unit and a second upper-layer interface unit~~,~~;

~~said~~ a communication path of ~~the~~ said ordinary ~~statement~~ data of said first encryption circuit ~~being connected~~ is coupled to said first upper-layer interface circuit~~,~~;

~~said~~ a communication path of ~~the~~ said ordinary ~~statement~~ data of said second encryption circuit ~~being connected~~ is coupled to said second upper-layer interface circuit~~,~~;

said first upper-layer interface unit ~~including~~ includes a first upper-layer communication path for communicating signals with a first upper-layer device outside said semiconductor chip~~,~~; and

said second upper-layer interface unit includes ~~including~~ a second upper-layer communication path for communicating signals with a second upper-layer device outside said semiconductor chip.

10. (Currently Amended) ~~An~~ The authentication communicating semiconductor device according to claim 8, further comprising an electrically rewritable nonvolatile memory formed on said single semiconductor chip, wherein said electrically rewritable nonvolatile memory ~~being connected~~ is coupled to said internal bus.

11. (Currently Amended) ~~An~~ The authentication communicating semiconductor device according to claim 7, wherein said lower-layer device is formed on said semiconductor chip, wherein said authentication communicating semiconductor device ~~further comprising~~ comprises ~~at least one~~ a communication path for communicating signals with said lower-layer device.

12. (Canceled).

13. An authentication communicating semiconductor device, comprising:

a semiconductor chip~~,~~:

a main processing unit ~~formed on said semiconductor chip~~ for generating a first key code according to a predetermined algorithm, for determining approval/non-approval of communication of data with an external device, and for controlling ~~the~~ said communication of data;

an encryption unit ~~formed on said semiconductor chip~~ for encrypting ~~and decoding~~ communication data ~~using~~ to transmit to an external device using ~~the~~ said first key code generated by said main processing unit; and

an interface unit ~~formed on said semiconductor chip~~ for ~~conducting~~ performing said communication of data with an upper-layer or a lower-layer according to a predetermined protocol,

wherein said main processing unit, said encryption unit and said interface unit are formed on said semiconductor chip,

wherein said encryption unit decodes communication data received from said external device using said second key code generated by said outside device,

wherein a standard of said interface is a predetermined standard, and

wherein said main processing unit, said encryption unit, and said interface units are coupled to each other via an internal bus.